IN THE CLAIMS:

1. (Previously presented) A deep trench capacitor in a monocrystalline semiconductor substrate, said capacitor comprising: (i) a buried plate in said substrate about an exterior portion of a trench in said substrate, (ii) a node dielectric about at least a lower interior portion of said trench, (iii) a trench electrode in said trench, and (iv) a conductive strap disposed between and electrically connected to the trench electrode and the monocrystalline substrate, said capacitor further comprising (v) a Si-C barrier layer containing silicon-carbon bonds that does not have the structure of silicon carbide between said monocrystalline substrate and said conductive strap, said Si-C barrier layer having been formed in the course of a plasma-assisted etch of an oxide layer adjacent to said monocrystalline substrate.

2. (original) The capacitor of claim 1, further comprising an oxide collar about an upper interior region of said trench and disposed below said conductive strap.

3. (cancelled)

4. (original) The capacitor of claim 1, wherein said Si-C barrier layer is located at an interface between said conductive strap and said monocrystalline substrate.

5. (cancelled)

6. (original) The capacitor of claim 1, wherein said Si-C barrier layer has a thickness of about 10nm.

7. (original) The capacitor of claim 1, wherein said conductive strap is a buried strap.

8. (original) The capacitor of claim 1, wherein said conductive strap comprises amorphous silicon.

9. (original) The capacitor of claim 1, wherein said trench electrode comprises doped polycrystalline silicon.

10. (original) The capacitor of claim 3, further comprising an additional Si-C barrier layer located at an interface between said conductive strap and said monocrystalline substrate.

11. (withdrawn) A method of forming a deep trench capacitor in a monocrystalline semiconductor substrate, said method comprising:

(a) providing a monocrystalline semiconductor substrate having (I) a buried plate about an exterior portion of trench in said substrate, (ii) a node dielectric about at least a lower interior portion of said trench, and (iii) a trench electrode in said trench;

(b) removing an upper portion of said trench electrode to provide space for a conductive strap, thereby exposing a trench electrode surface and a vertical substrate surface;

©) reacting, in the presence of an electric field, said exposed surface of the electrode and the substrate about said space with a compound containing carbon to form a Si-C barrier layer on at least said substrate surface; and

(d) filling said space over said electrode layer with a conductive strap material.

12. (withdrawn) A method according to claim 11, wherein said step of removing an upper portion is performed with a reactive ion etch on oxide and said compound containing carbon is the etchant gas.

13. (withdrawn) A method according to claim 12, wherein a power level of RF power is above a threshold value.

14. (withdrawn) A method according to claim 13, wherein said power level is maintained at the end of an oxide removal etching process.

16. (withdrawn) The method of claim 11, further comprising removing said Si-C layer from said trench electrode surface before step (d).

17. (withdrawn) The method of claim 11, wherein step ©) is performed at about 20 to 80 degrees Centigrade.

18. (withdrawn) The method of claim 11 wherein step (a) further comprises providing an oxide collar about an upper interior region of said trench, and step (b) further comprises removing a portion of said oxide collar and thereby exposes a vertical surface of said substrate.

19. (withdrawn) A method according to claim 18, wherein said step of removing an upper portion is performed with a reactive ion etch on oxide and said compound containing carbon is the etchant gas.

20. (withdrawn) A method according to claim 18, wherein a power level of RF power is above a threshold value.